

Improved Morphology and Performance from Surface Treatments of Naphthalenetetracarboxylic Diimide Bottom Contact Field-Effect Transistors

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ABSTRACT We report bottom contact organic field-effect transistors (OFETs) with various surface treatments based on n-channel materials, specifically, 1,4,5,8-naphthalene-tetracarboxylic diimides (NTCDIs) with three different fluorinated N-substituents, systematically studied with a particular emphasis on the interplay between the morphology of the organic semiconductor films and the electrical device properties. The morphological origins of the improvements were directly and dramatically visualized at the semiconductor-contact interface. As a result of a series of treatments, a large range of performances of bottom contact side-chain-fluorinated NTCDI OFETs (mobility from 1×10^{-6} to 8×10^{-2} $\text{cm}^2/(\text{V s})$, on/off ratio from 1×10^2 to 1×10^5) were obtained. The surface treatments enabled systems that had shown essentially no OFET activity without electrode modification activity to perform nearly as well as top contact devices made from the same materials. In addition, for the fresh bottom contact NTCDI device, the effect of gate bias stress on the tens-of-minutes time scale, during which the threshold voltage (V_t) shifted and relaxed with similar time constants, was observed.

KEYWORDS: organic thin film field-effect transistors (OFETs) • 1, 4,5,8-naphthalenetetracarboxylic diimides (NTCDIs) • atomic force microscopy (AFM) • morphology • interface • bias stress

INTRODUCTION

Organic thin film field-effect transistors (OFETs) have attracted considerable interest for use in a number of applications such as flexible active matrix displays, chemical sensors, radio frequency identification tags and labels, smart cards, and large-area logic circuits (1–6). One area where organic electronics holds significant promise is in very high altitude or space technology, where shape conformality may be useful, where weight minimization is imperative, and where radiation stability must be established. OFETs have been studied in two configurations, top contact and bottom contact. For top contact devices, shadow-masking techniques are normally used to pattern the source-drain electrodes because organic semiconductors are normally sensitive to solvents and chemicals used in photolithographic processing and OFET performance may be degraded when using traditional patterning methods in device fabrication (7). Therefore, bottom contact OFETs, constructed by patterning electrodes first and then depositing organic films in order to avoid or minimize their exposure to chemicals and solvents, are often preferred. Bottom contacts are also more desirable for radiation testing, to distinguish effects on the semiconductors from static charg-

ing of the dielectrics. However, it has been demonstrated that the bottom contact configuration often gives inferior performance to the top contact configuration for a wide variety of organic semiconductors because the contact area between the channel region of the semiconductor film and the source/drain electrodes is small. In this situation, the effects of surface dipoles, the insulating nature of the side chains on organic semiconductor molecules, or delamination of the semiconductors from the electrodes would be much more significant (8–11).

Surface modification of source/drain electrodes via adsorption of a polar thiol onto the gold prior to deposition of the semiconductor has been used to improve the physical connection between electrode and semiconductor channels, thereby enhancing the performance of bottom-contact devices. Historically, many reports have illustrated the characteristics of bottom contact OFETs based on p-channel materials such as pentacene, copper phthalocyanine (CuPc) and sexthiophene in which holes are the majority carriers (12–15). However, very few studies have investigated n-channel organic semiconductor growth on substrates with prepatterned OFET metal contacts, relevant to bottom-contact devices (16–18). The investigation and development of materials that can be used in n-channel organic transistors, particularly those that can be operated in air, is crucial for the development of practical organic electronics, such as the most power-efficient families of logic elements called “complementary” circuits, in which both hole-carrying (p-channel) and electron carrying (n-channel) semiconductors are required (19–23).

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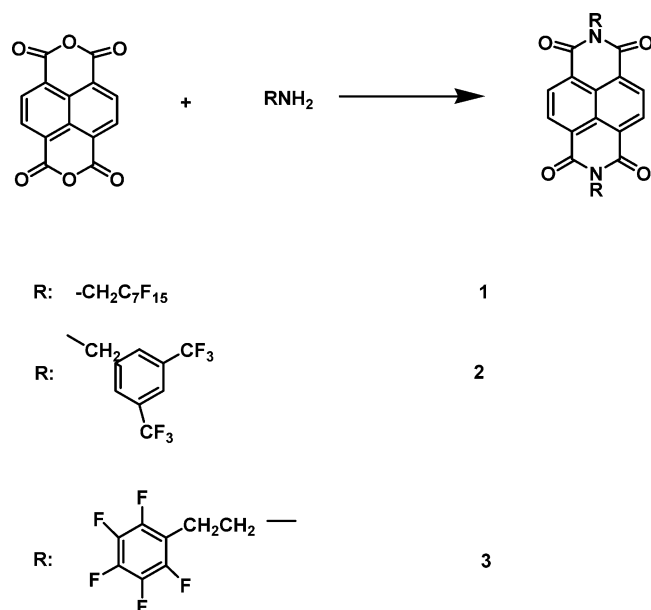


FIGURE 1. General synthetic route and structure of semiconductor molecules.

In 2000, Katz et al. reported a series of n-type materials, namely, 1,4,5,8-naphthalene-tetracarboxylic di-imides (NTCDIs), a class of condensed ring compounds that when N-substituted with fluorinated side chains (especially *N,N'*-bis (pentadecafluorooctyl) to make F15-NTCDI), are apparently stabilized to electron transport, with mobility up to $0.1 \text{ cm}^2/(\text{V s})$. This protection against electron quenching occurs even though the fluoro substitution on the side chains is far enough from the conjugated system to have little effect on the orbital energy levels (8, 24). A large number of additional NTCDI compounds with fluoro substitution were then synthesized, with mobility reaching $0.57 \text{ cm}^2/(\text{V s})$ (25–29). For most of these NTCDI studies, the top contact configuration was used. Very few studies have investigated bottom contact devices, and none have focused on film growth and semiconductor-metal-dielectric interface morphology (30).

In this present manuscript, we describe bottom contact OFETs with various surface treatments based on NTCDI derivatives with three different fluorinated N-substituents, systematically studied with a particular emphasis on the interplay between the morphology of the organic semiconductor films and the electrical device properties. The surface treatments enabled systems that had shown essentially no OFET activity without electrode modification activity to perform nearly as well as top contact devices made from the same materials. The morphological origins of the improvements were directly and dramatically visualized at the semiconductor–contact interface. In addition, bias stress effects in freshly prepared bottom contact devices were explored.

EXPERIMENTAL SECTION

Materials. NTCDI compounds **1**, **2**, and **3** (Figure 1) were synthesized with simple one-step procedures. Thiols 3-mercaptopropyltrimethoxysilane (MPTMS) and 4-chlorobenzenemethanethiol (98%) were obtained from Aldrich. 1H,1H,2H,2H-per-

fluorohexanethiol and 1H,1H,2H,2H-perfluorooctanethiol were ordered from Oakwood products Inc. Poly(Alpha-methylstyrene) $M_w = 5000$ was ordered from Polysciences. Hexamethyldisilazane (HMDS) was ordered from Aldrich. All of these purchased materials were used as received.

Substrates and Procedures. OFETs were fabricated by thermal evaporation of gold and organic films onto heavily n-doped silicon wafers including a 300 or 55 nm thermally grown gate oxide layer. Deposition took place under vacuum at pressure of 2×10^{-6} to 6×10^{-6} mbar at a rate of $\sim 0.5 \text{ \AA/s}$. A heated stage was used to maintain elevated substrate temperature during semiconductor deposition. For the device with silane monolayer modification, entire substrates were cleaned by piranha solution ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ 3:1; **caution!** highly oxidizing and corrosive) first and then treated with HMDS or MPTMS vapor for 2 h at $100 \text{ }^\circ\text{C}$. For the MPTMS treatment, reaction occurs between the SiO_2 surface silanols and the silyl group ($\text{Si}(\text{OCH}_3)_3$) of MPTMS with formation of covalent Si–O–Si bonds to the SiO_2 surface, leaving the thiol (–SH) functional group to react with gold electrode (31). For the device without silane modification, substrates were cleaned by acetone and isopropyl alcohol for 15 min. For the devices with aromatic thiol modification, thiols were deposited onto gold contacts in 0.1% ethanol solution at room temperature for 2 h. To fabricate bottom contact devices, we patterned Au electrodes through a shadow mask (channel length $250 \text{ }\mu\text{m}$, channel width $6000 \text{ }\mu\text{m}$), and the NTCDI was thermally evaporated after gold deposition and thiol treatment, if any.

Device Characterization. DC characteristics of the devices were obtained using a semiconductor parameter analyzer (Agilent 4155C). Output characteristics (plotted as square roots of saturated drain currents vs gate voltage) were obtained at a constant gate voltage $V_g = 100 \text{ V}$ and transfer characteristics at a constant drain voltage $V_{sd} = 100 \text{ V}$. The current I_D modulated by V_G is approximately determined from the following equation

$$I_D = (W/2L)C_i\mu(V_G - V_T)^2(\text{saturation regime}) \quad (1)$$

where μ is the field-effect mobility, L is channel length ($250 \text{ }\mu\text{m}$) and W is channel width (6 mm), C_i is the insulator capacitance per unit area, and V_T is the extrapolated threshold voltage. We used eq 1 to estimate μ by plotting $(I_D)^{1/2}$ versus V_G . “Mobility” here is an apparent mobility that may well be severely limited by contact resistance, and does not necessarily reflect the channel mobility along the length of the OFETs. Device parameters reported in the text for data in figures apply to those figures, which are individual examples from the sets of data listed in Table 1.

Bias Stress Test. Device characterization was carried out using an HP 4156 semiconductor parameter analyzer. Working in the saturation mode, a voltage of +15 V was applied between the drain and source contacts (V_{ds}) while the gate voltage (V_{gs}) was swept from 0 to +10 V. Plots were then made of the square root of the source-drain current ($(I_{ds})^{1/2}$) as a function of V_{gs} and the threshold voltage (V_T) extracted from the V_{gs} intercept of the linear region of the plot. For bias stress experiments, a fixed V_{gs} value was applied (15 V) for a chosen time and then the $I_{ds}(V_{gs})$ measurement performed. The source and drain contacts were shorted during the biasing step. This process was repeated. In this “stop/start” mode of bias/measurement the approximate time to stop the bias and complete the $I_{ds}(V_{gs})$ measurement was $\sim 5 \text{ s}$.

Atomic Force Microscopy (AFM) Measurements. The AFM measurements were performed with a Pico Plus scanning probe microscope (Agilent Co.) operated at room temperature. A silicon tip with spring constant of $\sim 0.05 \text{ N/m}$ and a scan rate

Table 1. Summary of Bottom Contact OFET Data

OSC	SiO ₂ layer thickness (nm)	surface modification on SiO ₂ substrate	Au film thickness (nm)	Au surface modification	organic film thickness (nm)	T _{sub} (°C)	no. of measurements	μ (cm ² /(V s)) ± std. dev.	current on/off
1	300	N/A	50	N/A	50	80	20	N/A	N/A
2	300	N/A	50	N/A	50	100	6		
3	300	N/A	50	N/A	50	100	5		
2	300	N/A	40	N/A	60	100	5	(7 ± 2) × 10 ⁻⁶	1 × 10 ² to 1 × 10 ³
1	300	MPTMS	50	HS-(CH ₂) ₂ -(CF ₂) ₅ -CF ₃	50	80	6	(3.2 ± 1.3) × 10 ⁻⁴	1 × 10 ² to 1 × 10 ³
1	300	MPTMS	50	HS-(CH ₂) ₂ -(CF ₂) ₅ -CF ₃	50	80	5	(1.9 ± 0.2) × 10 ⁻⁴	1 × 10 ² to 1 × 10 ³
1	300	MPTMS	50	4-chlorobenzene-methanethiol	50	80	4	(1.5 ± 0.2) × 10 ⁻³	1 × 10 ² to 1 × 10 ³
1	300	MPTMS	50	N/A	50	80	6	(2.0 ± 0.3) × 10 ⁻³	1 × 10 ³ to 1 × 10 ⁴
1	300	MPTMS	50	4-trifluoromethylbenzyl mercaptan	50	80	15	(2.8 ± 1.3) × 10 ⁻²	1 × 10 ³ to 1 × 10 ⁵
2	55	MPTMS	50	N/A	50	100	4	(4.9 ± 0.3) × 10 ⁻³	1 × 10 ⁴ to 1 × 10 ²
2	55	MPTMS	20	HS-(CH ₂) ₂ -(CF ₂) ₅ -CF ₃	100	100	8	(7 ± 0.6) × 10 ⁻²	1 × 10 ³ to 1 × 10 ⁴
2	300	Cr/HMDS	20	HS-(CH ₂) ₂ -(CF ₂) ₅ -CF ₃	100	100	7	(1.0 ± 0.2) × 10 ⁻²	1 × 10 ² to 1 × 10 ³
3	300	poly-α-methyl styrene	30	N/A	100	100	6	(2.5 ± 0.2) × 10 ⁻²	1 × 10 ⁴ to 1 × 10 ⁵
2	300	poly-α-methyl styrene	30	N/A	100	100	7	(1.8 ± 0.4) × 10 ⁻²	1 × 10 ³ to 1 × 10 ⁴

of 1 Hz were used. All AFM measurements were carried out in the contact mode.

RESULTS AND DISCUSSION

Bottom contact OFETs without any thiol treatment were first fabricated (50 nm organic film **1**, **2**, **3**/50 nm Au/300 nm SiO₂/p-doped Si) and tested under air or vacuum (Figure 2a), with no device showing n-type transistor behavior. However, for top contact OFETs (50 nm Au/50 nm organic film/300 nm SiO₂/p-doped Si), n-channel activity was obtained just as previously reported (8, 28, 29). To understand the reason for the inactivity of the bottom contact devices, the topography of the compound **1** bottom contact device without any surface treatment was first characterized by AFM. Figure 2b shows AFM images of 50 nm compound **1** deposited on SiO₂ after 50 nm Au film deposition within the channel region and on the Au electrode. It can be seen that a fairly unstructured organic film has grown on top of the gold electrodes whereas a terrace crystal structure was formed on the bare silicon substrate. At the interface area between the bare SiO₂ substrate and the Au electrode, a clear “gap” can be observed. The organic film far away from the “gap” area consists of fairly large terraced grains (having sizes over 1 μm) (Figure 2c). On the other hand, for the organic film close to the “gap” area, the size of terrace grains decreased (from 1 μm to 200 nm), and the morphology of the organic film became more disordered at the gap area, with a higher density of defects such as pinholes and grain boundaries (Figure 2d). For the organic film grown on the gold electrode, an irregular film with roughness around ~15 nm can be observed (Figure 2e). In summary, the morphologies on the bare SiO₂ and on/near the gold electrodes are very different in morphology and continuity, and this is almost certainly the source of the performance limitation of the bottom contact device.

Thiol and Silylthiol Surface Treatments. A simple and flexible method to improve charge injection would be to cover gold surfaces with an aromatic thiol. However, thiol solutions tended to cause delamination of the Au electrode after more than a few minutes, because of the lack of a metal

glue layer (8). One way to improve the adhesion of Au electrode on substrates is first to grow self-assembled monolayers on the silicon substrate. MPTMS was selected as the glue layer between bare SiO₂ and Au electrodes. The adhesive stability of the MPTMS/Au layer was tested by dipping the sample in different aromatic thiol solutions for 12 h and cleaning with ethanol. In these tests, the Au layer was unaffected (no crack or delamination is observed by optical microscopy). We then proceeded to form OFETs. Figure 3a shows the schematic of a compound **1** device with MPTMS treatment. AFM images of the device are shown in Figure 3b. It can be observed that the relatively unstructured film was still grown on top of the gold electrodes and the terrace crystal structure was formed on the silicon substrate. However, compared to the AFM image of the untreated F15-NTCDI device, it is very difficult to detect any “gap” area at the interface between SiO₂ and the Au electrode (Figure 3b). Further zooming in on the interface area, it can be seen that a film of larger crystallites (below 1 μm) grew on the MPTMS/SiO₂ substrate far from the interface area (Figure 3c) and smaller size crystallites formed close to interface layer. Otherwise, it is very difficult to observe a distinct morphology boundary (heterogeneous interface) at the interface region between MPTMS/SiO₂ substrate and Au electrode (Figure 3d). For the organic film grown on the gold electrode, a more irregular film can be observed (Figure 3e). From the AFM images, it can be seen that the MPTMS monolayer not only serves as a glue layer between the Au electrode and SiO₂ substrate, but also alleviates the morphology limitation of the NTCDI bottom contact device. Panel b shows characteristics of a bottom contact OFET based on 50 nm compound **1**-50 nm Au-MPTMS-SiO₂/Si. From the curve of the square root of the drain current versus gate voltage at a constant 100 V drain-source voltage, carrier mobility is estimated to be 2.3 × 10⁻³ cm²/(V s) and the on/off ratio is 1 × 10⁴. The same method was also used for compound **2**-based bottom contact device fabrication. A 50 nm compound **2**-50 nm Au-MPTMS-54 nm SiO₂/Si device was fabricated, and it showed

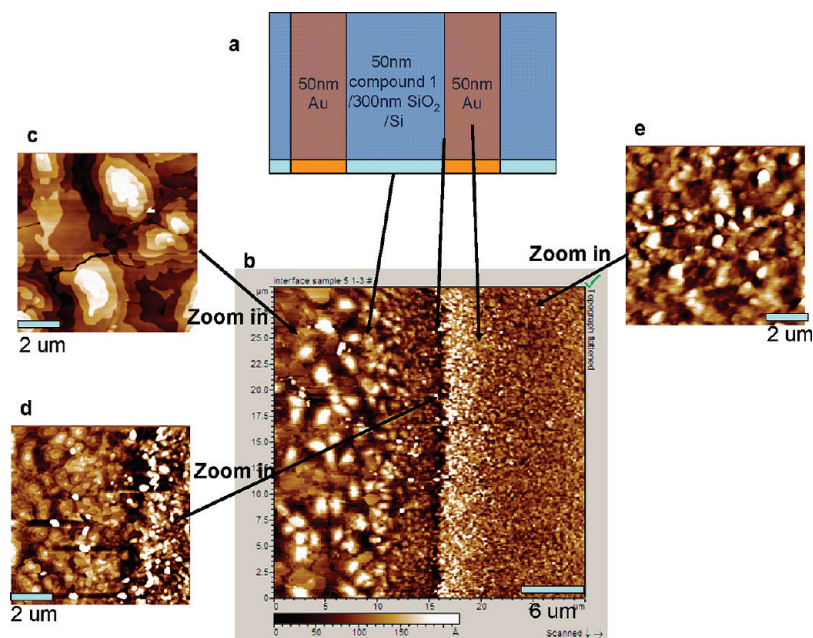


FIGURE 2. (a) Schematic of device structure for compound 1 bottom contact device without surface treatment; (b) AFM image of interface area of compound 1 on SiO₂ substrate and Au electrode; (c) zoomed in AFM image of compound 1 on SiO₂ substrate; (d) zoomed in AFM image of interface area of compound 1 on SiO₂ substrate and Au electrode; (e) zoomed in AFM image of compound 1 on Au electrode.

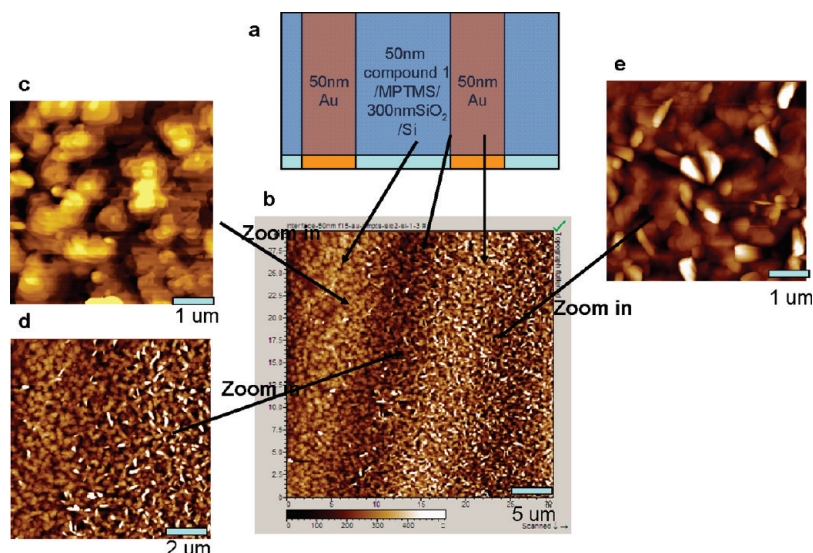


FIGURE 3. (a) Schematic device structure of bottom contact of compound 1 device with MPTMS surface treatment; (b) AFM image of interface area of compound 1 on MPTMS/SiO₂ substrate and Au electrode; (c) zoomed in AFM image of compound 1 on MPTMS/SiO₂ substrate; (d) zoomed in AFM image of interface area of compound 1 on MPTMS/SiO₂ substrate and Au electrode; (e) zoomed in AFM image of compound 1 on Au electrode.

n-type transistor behavior with mobility of $\sim 5.2 \times 10^{-3} \text{ cm}^2/(\text{V s})$ and on/off ratio of 1×10^2 .

To further improve the performance of NTCDI bottom contact OFETs, other aromatic thiols were used to modify the Au electrodes. Panel d of Figure 4 show characteristics of a bottom contact OFET based on 50 nm compound 1-4-trifluoromethylbenzyl mercaptan-50 nm Au-MPTMS-SiO₂/Si. From the curve of the square root of the drain current vs. gate voltage, mobility is determined to be $4.1 \times 10^{-2} \text{ cm}^2/(\text{V s})$, almost the same as that of the top contact device.

Semiconductor–Electrode Thickness Ratios. Besides surface treatments to improve bottom contact device performance, optimized contact geometry can also help

ensure good charge injection and low contact series resistance. One way to optimize the geometry of a bottom contact device is to adjust the semiconductor/conductor thickness ratio. The impact of semiconductor/conductor metal thickness ratio on pentacene -based p-type bottom contact OFETs has been reported recently (32). For the bottom contact NTCDI fluoro derivative OFET, increasing the thickness of the organic film and decreasing the thickness of the Au electrode (without affecting the Au electrode conductivity) help to minimize the effective contact resistance and improve organic film coverage on the Au bottom contact (panels a and b in Figure 5). A series of compound 2-based bottom contact devices with different organic film/Au

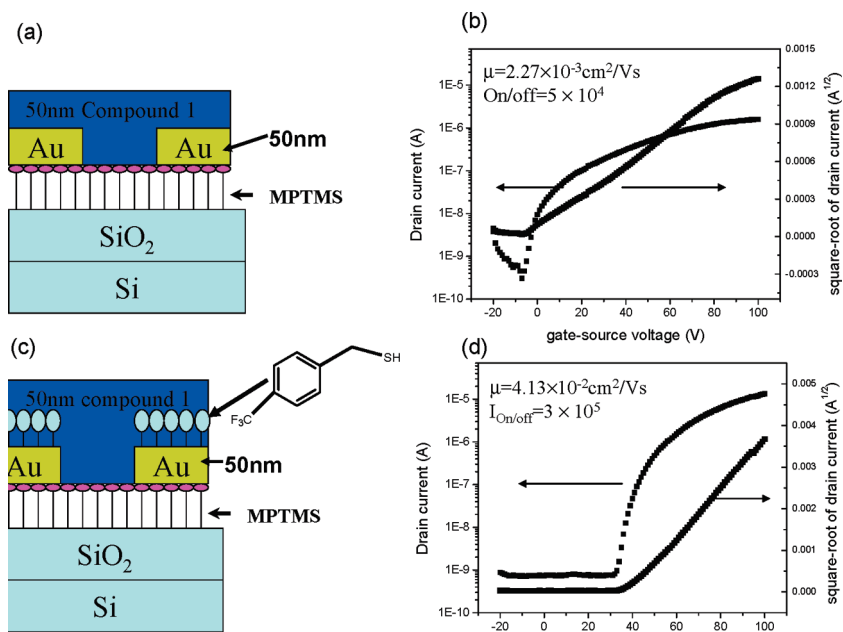


FIGURE 4. (a, b) Schematic device structure and characteristics of compound 1 device with MPTMS treatment; (c, d) schematic device fabrication and output characteristic of compound 1 device with MPTMS and aromatic treatment.

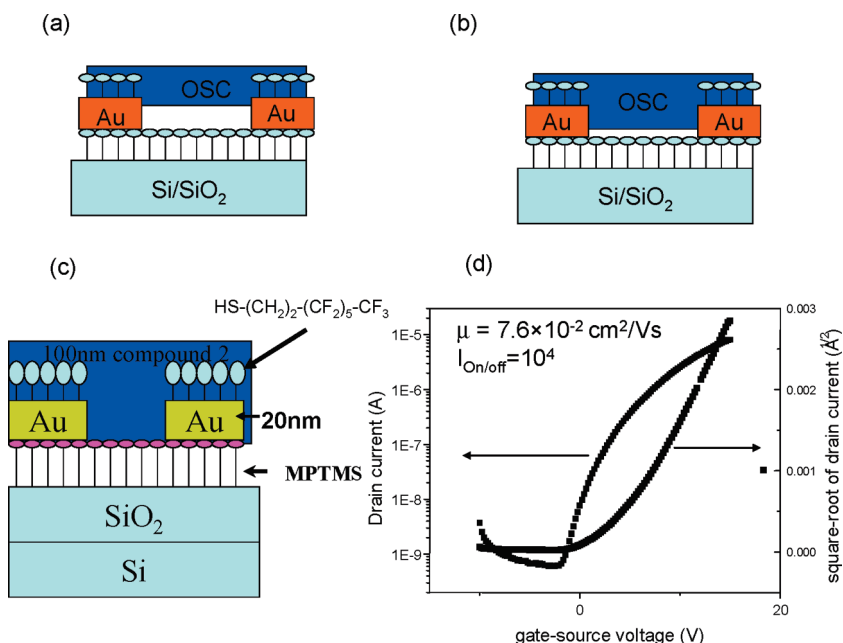


FIGURE 5. (a) Schematic graph for bottom contact device structure with low organic film/Au thickness ratio; (b) schematic graph for bottom contact device structure with high organic film/Au thickness ratio; (c, d) schematic device structure and characteristics of bottom contact compound 2 device.

thickness ratios were fabricated and tested. The 60 nm compound 2 film/40 nm Au/300 nm SiO₂/p-doped Si device (organic film/Au thickness ratio = 1.5 and without any surface treatment) showed marginal n-type transistor behavior with measured mobility of $\sim 8.4 \times 10^{-6} \text{ cm}^2/(\text{V s})$ and on/off ratio of 1×10^2 . Improvement of the bottom contact device was obtained by combining surface treatment and optimized thickness ratio of the organic film and Au electrode, as shown schematically for compound 2 along with device characteristics in panel d in Figure 5. The field-effect mobility calculated from the saturated region is $7.8 \times 10^{-2} \text{ cm}^2/(\text{V s})$ with a corresponding on/off ratio of 1×10^4 . This

combined approach represents the most dramatic improvement so far.

Interfacial Polymers on the Dielectric Interface. Because SAM preparation normally is time consuming and some SAM-forming thiols have unpleasant odors, we also investigated an alternative means of improving this near-contact NTCDI morphology without SAM modification, namely, spin coating a thin layer of insulating polymer on the gate-gate dielectric substrate. Thus we combined compound 2 or 3 and a spin-coated thin layer of poly- α -methylstyrene ($\sim 20 \text{ nm}$ thickness) on the usual Si/SiO₂ substrate for top contact device fabrication and acquired exceptionally

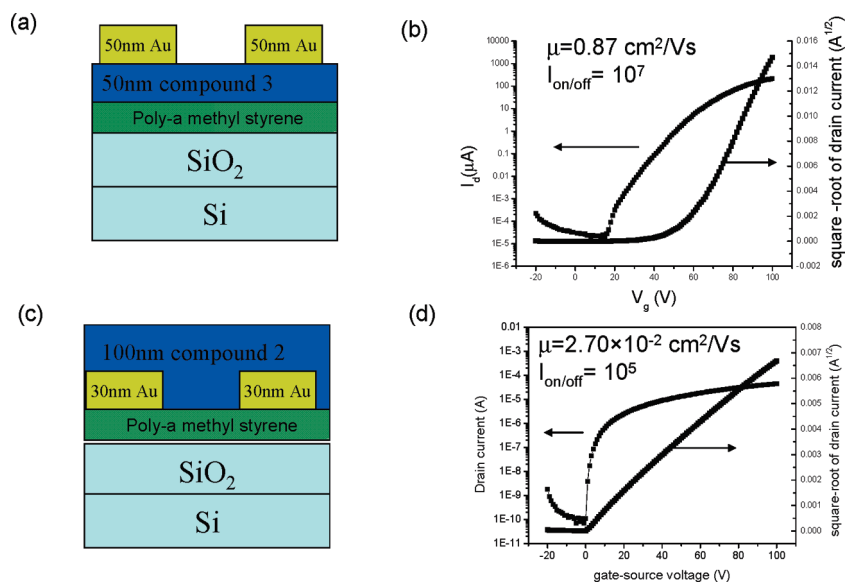


FIGURE 6. (a, b) Schematic device structure and output characteristic of top contact compound 3 device with insulating polymer treatment; (c, d) schematic device structure and characteristics of top contact compound 2 device with insulating polymer treatment.

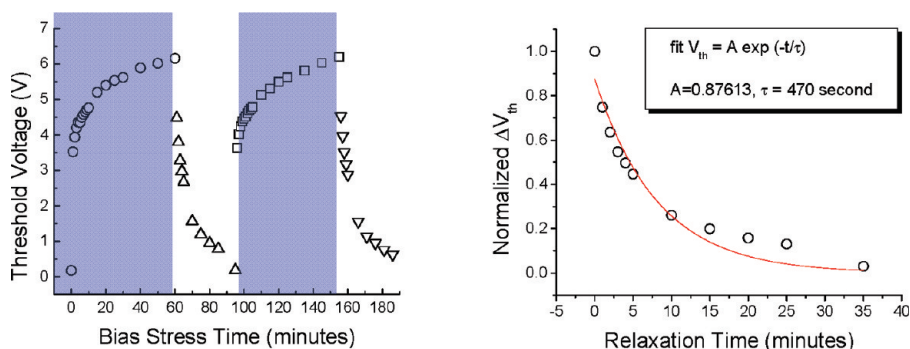


FIGURE 7. Dependence of the V_t shift on the stress time for fresh 100 nm compound 2/H₂S-(CH₂)₂-(CF₂)₅-CF₃/20 nm Au/MPTMS/55 nm SiO₂/Si OFET under a continuous gate bias stress (~ 3 MV cm⁻¹) and then relaxed under no bias (all terminals shorted). Left: V_{th} versus time for two cycles of bias stress followed by relaxation (blue region, bias potential +15 V; blank region, bias potential 0 V). Right: First relaxation cycle plotted on an expanded x-axis. The second relaxation is essentially identical.

high quality characteristics. Panels a and b in Figure 6 show the schematic graph for top contact device fabrication and transfer and output characteristic for compound 3. Mobility is determined to be 0.87 cm²/(V s), almost the same as that of hydrogenated amorphous silicon. Panels c and d in Figure 6 show a schematic graph for bottom contact device fabrication and characteristics, in this case for compound 2. The carrier mobility is 2.7×10^{-2} cm²/(V s) and on/off ratio is 1×10^4 . A 100 nm compound 3-30 nm Au-20 nm poly α -methylstyrene-300 nm SiO₂/Si device was fabricated and it showed n-type transistor behavior with mobility of $\sim 2.2 \times 10^{-2}$ cm²/(V s) and an on/off ratio of 1×10^5 .

Table 1 summarizes the series of NTCDI derivatives (compound 1, 2, and 3) in the bottom contact devices, reporting averages of devices made under conditions discussed above. From the various combinations of surface treatments such as aromatic thiol treatment of Au electrode, HMDS, MPTMS, or poly α -methylstyrene treatment of the Si/SiO₂ substrate, and optimized ratio of organic film and Au film thickness, a large range of performances (mobility from 1×10^{-6} to 8×10^{-2} , on/off ratio from 1×10^2 to 1×10^5) were obtained.

Effect of Bias Stress. To understand the stability of NTCDI bottom contact devices, one of the most important issues is the effect of gate bias stress, during which the threshold voltage (V_t) tends to shift under a continuous gate bias (33). Gate bias stress measurements were performed in dry air (humidity < 20 %). Typically, ca. 3 MV cm⁻¹ across the dielectric/source-drain shorted was applied on an OFET for 1 hr. After recovery of the transistor (with gate/source/drain all shorted), the measurement was repeated. Figure 7a shows the dependence of the V_t shift on the stress time for a fresh 100 nm compound 2 /H₂S-(CH₂)₂-(CF₂)₅-CF₃/20 nm Au/MPTMS/55 nm SiO₂/Si bottom contact device, corresponding to a superior bottom contact OFET. There is a positive threshold shift consistent with negative charge trapping and there is a fast relaxation phenomenon after biasing (cycling charging/discharging). The relaxation time τ can be acquired by fitting the relaxation curve after biasing, as shown in Figure 7b. Using a simple exponential decay equation ($V_t = A \exp(-t/\tau)$), we obtain $\tau = 470$ s. Thus, there are electron traps that fill and then empty on the minutes time scale. Switching at frequencies >1 HZ and observation

of radiation effects on the seconds time scale should not be affected by bias stress observed here.

The trap depth of the OFET device can be determined by the following (34)

$$\tau = \nu^{-1} \exp(E_a/k_B T) \quad (2)$$

where E_a is the mean activation energy for detrapping, ν is a frequency prefactor (typical ranges for ν are $1 \times 10^{10} < \nu < 1 \times 10^{12} \text{ S}^{-1}$), T is 300 K, and τ is the relaxation time.

From this equation, the trap depth in the OFET can be estimated to be between 0.76 eV to 0.88 eV. There are multiple ways to explain this trap depth. One possibility is that this trap depth reflects the energy difference between the carrier orbitals in the molecules and the lowest unoccupied orbital of molecular oxygen. We do observe that long-term storage of the device in air leads to a larger initial threshold voltage. Another possibility is that there is some trap at the measured depth at the dielectric interface. Finally, there could be some unknown impurity responsible for the trap, though the material used has been sublimed for purification and then again during deposition.

CONCLUSIONS

In this study, a series of side-chain-fluorinated NTCDI-based bottom-contact OFETs have been prepared and characterized with a particular emphasis on the interplay between the morphology of the organic semiconductor films and the electrical device properties. The growth of NTCDI films on Si/SiO₂ substrates is dominated by crystalline grain structures; however, their growth on bare gold is dominated by a dewetting resulting in a rough and amorphous film. A clear “gap” is formed at the interface between Si/SiO₂ and Au substrates. To overcome the morphology limitations, different methods were studied: (1) surface chemical modifications of Au electrode and Si/SiO₂ substrates are applied to improve the morphology in the OFET channel close to the electrode edge and (2) semiconductor-contact thickness ratios are optimized to allow charge injection through larger interface areas. A large range of performances of bottom contact side-chain-fluorinated NTCDI OFETs (mobility from 1×10^{-6} to $8 \times 10^{-2} \text{ cm}^2/(\text{V s})$, on/off ratio from 1×10^2 to 1×10^5) were obtained. In addition, effect of gate bias stress on the tens-of-minutes time scale, during which the threshold voltage (V_T) shifted and relaxed with similar time constants, was observed.

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